In the Specification:

[0042] FIG. 10 is provided to illustrate that during 1149.1 data scan operations the TLM is configured, as described in regard to FIG. 8A, to simply form a connection path between the output of the selected TAP domain arrangement 901-907 and the IC's TDO pin. Thus the TLM does not add bits to 1149.1 ~~instruction~~ data scan operations as it does for 1149.1 instruction scan operations. The forming of a connection path through the TLM during data scan operations is disclosed in the referenced pending patent application Ser. No. 091277,504, filed Mar. 26, 1999.